REMARKS

Claims 1-51 were pending in this Application. Claims 18-51 were withdrawn from consideration in response to an earlier restriction requirement, and are canceled in this Response. (Applicants reserve the right to pursue these claims in a divisional application.) Claims 1-17 were examined and stand rejected. In this Response, Applicants amend claims 1 and 11, and add new claims 52-57, without adding any new matter. Support for the amendments and new claims is at [0061], [0071], Figure 2, elements 30 and 42; and Figures 6 and 7. Reconsideration in light of the following remarks is requested.

I. Claims Rejected Under 35 U.S.C. § 103(a)

The Examiner rejected claims 1-17 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,343,339 issued to Daynes ("*Daynes*") in view of *Structured Computer Organization* by Andrew S. Tannenbaum ("*Tannenbaum*"). However, the references of record fail to teach or suggest at least the newly-added element of the rejected claims, and so the claims should be patentable over the references.

As a preliminary matter, it should be pointed out that *Tannenbaum* merely states a general principle, that hardware and software are logically equivalent: operations performed in software can be built into and performed by hardware, and vice versa. However, this general principle fails to provide motivation for selecting a software or hardware implementation of a particular function. The Examiner asserts that it would have been obvious to one of ordinary skill to implement *Daynes*'s software semaphores in hardware, "in order to realize benefits in cost, speed and reliability." But neither *Daynes* nor *Tannenbaum* identify a problem with the speed of software semaphores or the cost of hardware semaphores that might invite one of ordinary skill to prefer one approach or the other. In fact, *Tannenbaum* does not even state a general rule

relating the factors of "cost, speed, reliability, and frequency of expected changes" to the choice of implementation style. Thus, although there may be reason to believe that a software semaphore implementation could be replaced by hardware offering similar functionality, there is no suggestion or motivation to try doing so. The rejections fail for at least that reason.

Turning now to the substance of the amended claims, claim 1 recites a processor for offloading processing in a storage environment comprising several elements, including a zero bus turnaround ("ZBT") interface that interfaces said processor to a network processor configured to perform a storage function. The Examiner asserts that *Daynes* teaches structures and logic to perform the claimed semaphore operations, and relies on *Tannenbaum*'s observation that "hardware and software are logically equivalent" to construct a *prima facie* case of obviousness. However, leaving aside the questions of whether *Daynes* may properly be combined with *Tannenbaum* and whether adequate motivation exists for implementing some of *Daynes*'s logical operations in hardware instead of software, neither reference teaches or suggests the specific hardware implementation claimed (a ZBT interface between the claimed processor and a network processor). Consequently, claim 1 is patentable over the references of record. The Examiner is respectfully requested to withdraw the rejection of this claim.

Claims 2-10 depend directly or indirectly on claim 1, and are patentable for at least the reasons discussed above. The Examiner is respectfully requested to withdraw the rejections of these claims also.

Claim 11 recites a method of controlling a processor for offloading processing in a storage environment comprising several steps, including receiving a signal from a network processor configured to perform a storage function through a zero bus turnaround ("ZBT") interface. As explained above, even assuming (solely for the sake of argument) that *Daynes* and *Tannenbaum* teach or suggest every element of the claimed method, and that the references

could properly be combined, the amended claim requires the signal to arrive through a ZBT interface, a feature that is absent from both references. Therefore, claim 11 is patentable over those references, and the Examiner is respectfully requested to withdraw this rejection.

Claims 12-17 depend directly or indirectly on claim 11, and are patentable for at least the reasons discussed above. The Examiner is respectfully requested to withdraw the rejections of these claims.

II. New Claims

New claim 52 recites a storage server comprising several elements, including a network processor to control routing of data frames into and out of the storage server and a co-processor to offload some functions performed by the network processor, the co-processor to communicate with the network processor via at least one interface, wherein the co-processor is to receive a command to release a semaphore from the network processor and return a release acknowledgement response if a thread is waiting for the semaphore.

This claim is believed to reflect the embodiment depicted in Figure 2 and salient aspects of its operation as explained with reference to Figure 7, and further to distinguish the claimed material from the references of record. For example, as the Examiner applies *Daynes*, the elements that allegedly read on the claimed network processor and co-processor are at opposite ends of the Internet, and could only communicate via the network. Yet the claim requires both the network processor and co-processor to be components of a (single) storage server, and the network processor to control routing of data frames into and out of the storage server. Even crediting the improbable assertion that one of ordinary skill would take *Daynes*'s processor 113 and server 126 to be sub-components of a single storage server that somehow includes the entire Internet within its boundaries, it is clear that server 126 does not control routing of data

frames into and out of the storage server, as the claim recites. For at least these reasons, the Examiner is respectfully requested to allow claim 52.

Claims 53 and 54 depend upon claim 52, and further refine the storage server described therein. It is respectfully submitted that these claims are allowable for the reasons discussed above, and also because the references of record fail to discuss material even tangentially related to the subject of these claims.

New claim 55 recites a method comprising several operations, including receiving a semaphore operation command from a network processor through an intra-system interface, the command to identify one of a plurality of semaphores; updating a data structure in a memory according to the semaphore operation command; and returning a semaphore operation result to the network processor through an intra-system interface, the result to indicate an outcome of the command. These operations are described in ¶¶ [0076]-[0094], in reference to Figures 6 and 7. In particular, Applicants call the Examiner's attention to the claim element requiring the semaphore operation from the network processor to be received *through an intra-system interface*, and the result to be returned *through an intra-system interface*. Figure 2 shows these interfaces as elements 40 and 42, and dependent claim recites the added limitation that an interface must be a zero bus turnaround ("ZBT") interface, exactly as shown in the Figure.

Passing commands and results over an intra-system interface is significant because, in the Examiner's analysis where a software-only semaphore manager operates, semaphore commands and results exist only as transient states within a processor executing the software; no identifiable command or result passes through an intra-system interface. Such communication is a feature of a hardware co-processor implementation of an offloaded software function. Applicants respectfully recall to the Examiner's attention the argument advanced above, that although *Tannenbaum* indicates generally that software and hardware implementations of a function are logically equivalent, there is no

teaching or suggestion in the references of record to select *semaphore operations* in particular as a useful or favorable function to implement in hardware with a co-processor.

CONCLUSION

In view of the foregoing, it is believed that all claims now pending, namely claims 1-17 and 52-57, patentably define the subject invention over the prior art of record, and are in condition for allowance and such action is earnestly solicited at the earliest possible date. If the Examiner believes that a telephone conference would be useful in moving the application forward to allowance, the Examiner is encouraged to contact the undersigned at (310) 207-3800.

Respectfully submitted,
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